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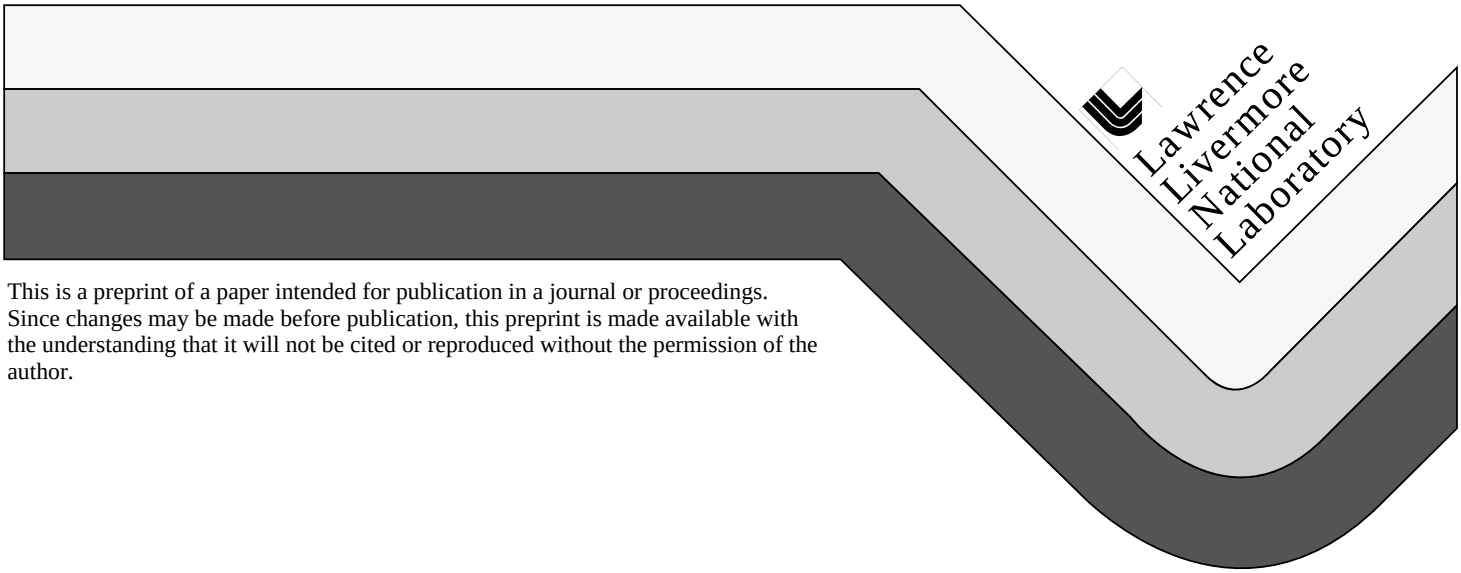

Fabrication of a DRAM Cube Using a Novel Laser Patterned 3-D Interconnect Process

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Abstract

A new process is described for producing metal interconnect on three dimensional surfaces. The process makes use of a laser to expose an electrophoretic photoresist which is conformally plated onto a thin metal seed layer that covers the various surfaces. After resist exposure and development, copper, nickel, and gold are plated onto the seed layer through the resist mask. Finally, the residual resist and seed layer are removed leaving conformally plated metal traces.

The process has been applied to the reroute of the I/O pads of DRAM chips to form new pads on one of the long sidewalls of the bare die. Die are stacked and bonded and pads are arranged so that data lines and some control lines in a stack are staggered while address, power, ground, and some control lines are positioned identically. This architecture permits bonding of the stack to a single sided flex tape using an anisotropically conducting adhesive. The flex is bonded to a circuit board to complete the assembly. The DRAM stack fabrication and attachment process is relatively simple and may be attractive for high density 3D packaging for consumer electronics.

Key Words: Laser patterning, vapor deposited polyimide, memory stacks, 3D packaging

Introduction

Packaging integrated circuits in three dimensions remains an important area of endeavor in the multichip module community. Many technologies have been proposed and demonstrated in the past decade.[1, 2, 3, 4] Impressive solid state recorders featuring 3D stacks as integrated memory components in a high performance multichip module system have been demonstrated, and very high density 3D stacks (> 40 chips/6 mm thick stack) have been produced.

A major drawback of a full implementation of any of the various 3D technologies has been the cost of the packaging.[4] The need for simpler, lower cost options to current technologies is the driving force behind the research and development in the high density IC packaging arena.

In the present work a 3D direct write laser lithography process is used to reroute pads on DRAM die to new pads on one of the long sidewalls of the die. Most lithographic techniques are inherently two dimensional - flat substrates are exposed by projecting light through flat masks, creating accurate patterns in the x and y axes only. Maskless laser direct writing overcomes the two dimensional nature of photolithography: a focused laser beam simply forms a point or image in space which can be made to coincide with the surface of the part. The laser apparatus is described in the following section.

Laser lithography requires a resist which will undergo chemical or physical change under the influence of the laser beam. Conventional resist is not a viable candidate for 3D patterning, because a conformal, uniform coating cannot be obtained on a complex surface by spinning or spraying. Electrodeposited photoresist (EDPR),[5] which is an aqueous micellar solutions of resist with minimal organic solvent and low solids content, can be electrochemically coated onto conductive surfaces with complicated topologies. With a positive EDPR, the laser-exposed areas are developed away, leaving openings in the resist through which copper,

nickel, and gold can be plated. After plating, the resist is stripped, and the seed layer is removed.

The present process is simpler than the earlier ones. For example, the present process avoids the sidewall polishing and metallization steps of references 2 and 3 and the pad bumping and TAB attachment in reference 1 and the corresponding wire bonding step in references 3.

Solder bump bonding has generally been used to attach die stacks to boards. Pad-to-pad cube attachment requires precise spacing between pads on different die which restricts tolerances on die thickness and die spacing. Thermal expansion of the cube must also be matched to that of the substrate to avoid solder bump stress failure.[2] In many cases the cube must be bonded to a TCE-matched carrier which provides a mechanical and electrical interface to the PCB.

A much more forgiving and simpler strategy has been adopted in this work. Following the stacking of the die, cubes are bonded to single sided flex tape using anisotropically conducting adhesive (ACA). A relatively low line count flex can be used because most of the I/O on a DRAM are intended to be bussed with corresponding I/O on other DRAM. In particular, address, ground, power, and some control lines are bussed on each cube; the data lines and other control lines are not bussed. The stack can be tested on the flex before it is connected to the next level of packaging. After test, the flex is bonded to an FR-4 PCB with the same ACA. The flex and ACA easily accommodate mechanical strain and die/adhesive non-uniformity is unimportant for these pad-to-line connections. Furthermore, edges of the die in a stack do not have to be precisely coplanar because of the flexibility of the flex and the method used to bond it to the stack (see below).

Laser Direct Write Apparatus

The laser exposure tool is shown schematically in Fig. 1. An argon-ion laser operating in the multiline UV range from 338 to 364 nm is used as the light source. The laser can be diverted along either of two beam paths, one normal to the surface, and the other at a 30° angle to the surface. An acousto-optic modulator (AOM) is used to change the laser power, and as a fast electronic shutter. The incident laser power is 6-20 mW, with a beam size of 6 µm x 35 µm (a cylindrical lens is used to focus the beam to a line, and an aperture is employed which allows the long dimension of the beam to vary from 5 to 65 µm).

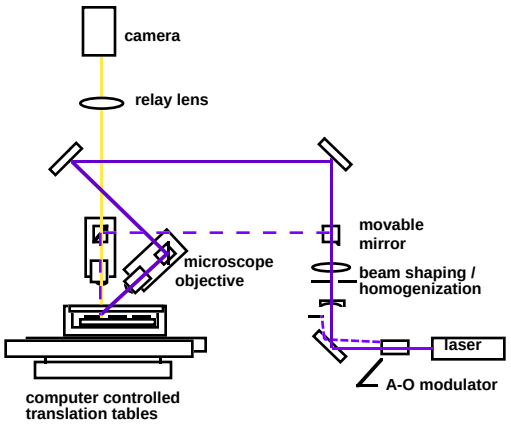

Figure 1: Laser direct write apparatus permits irradiation of vertical and horizontal die surfaces

UV microscope objectives are used to focus the laser beam after the cylindrical lens. These objectives are fixed, and a z-axis translation stage is used to focus the beam by moving the sample with respect to the objectives. A mirror mounted on a computer controlled stepper motor is moved into the beam path to direct the beam through the angled or normal objectives. A monitoring lamp directed through the normal objective by means of a beam splitter onto both the substrate surface and into a camera allows the operator to both register the die with respect to the substrate, and to watch the laser rastering on the surface.

Laser Metallization Process

The individual die are temporarily bonded to a silicon wafer carrier, allowing the die to be processed in a batch for greater efficiency. Following die attachment to the carrier, a conformal dielectric coating is applied in order to passivate the sidewalls of the chip. Two dielectric processes have been used for this passivation step. One process uses a vapor deposited polyimide coating which is easily ablated from the bond pads before metallization.[6, 7] A second process uses PECVD silicon oxide. The SiO_2 process is both reliable and cost effective when applied to die with bond pads in the center of the chip, because a shadow masking technique can be used to keep the bond pads clear of SiO_2 during deposition, eliminating

the necessity of another processing step to open the vias. For chips with bond pads arrayed along the periphery, the VDP polyimide process is preferred.

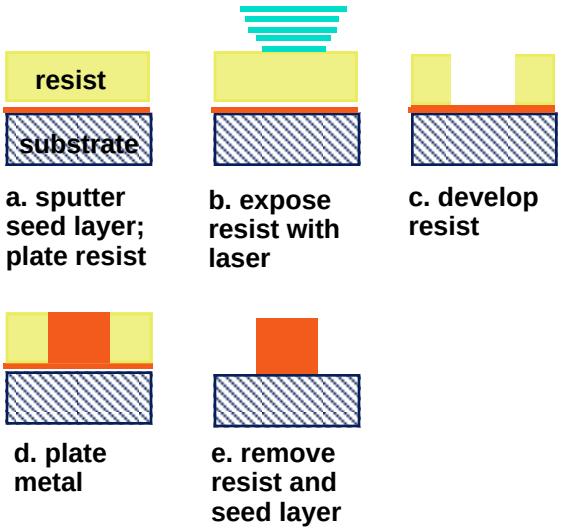

Figure 2: 3D direct write process sequence for positive resist.

After the die have been passivated, a metal seed multilayer is deposited everywhere (see Fig. 2), and positive EDPR is electroplated onto the module. The EDPR is exposed with the computer controlled laser patterning apparatus, and the resist is developed. Copper is then electroplated in the developed areas (through-the-mask-plating), forming the metal interconnects, and Ni and Au are electroplated on top of the copper. The EDPR is stripped to reveal the metal seed layer below, which is then etched away (the seed layer is ≤ 4% of the interconnect thickness, so the thickness of the interconnect lines are not substantially reduced by the seed layer removal). The resultant metal traces are rugged and reliable. They can be produced in thicknesses ranging from 2 µm to 10 µm, depending on the electrical requirements. An SEM of a metal trace at the edge of a 1 Mb DRAM die is shown in Fig. 3. No substantial thinning or defects are observed in the traces at the edge. Trace thickness is 5 µm and width at the edge of the die is 25 µm.

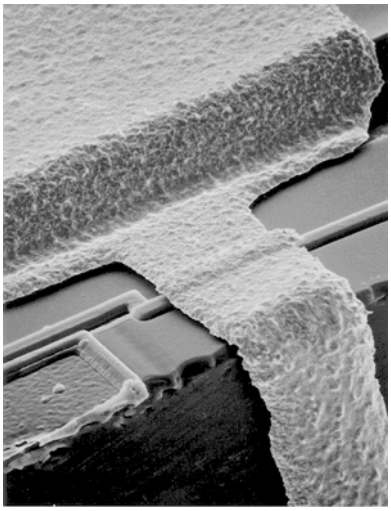

Figure 3 A trace at the edge of a 1 Mb DRAM chip appears as robust as on flat surfaces. Trace thickness is 5 µm and width at the edge is 25 µm.

Application of Laser Writing to Dense Solid State Memories

Using the laser patterning process, it is relatively simple to reroute contacts on DRAMs or other integrated circuit chips from the front face to the sidewall of the die so that the die can be stacked with other die and connected to the next level of packaging. Fig. 4 shows a 16 Mb DRAM with pads near the median of the die. Using the laser process, the pads have been rerouted to one edge of the die. The pads formed on the sidewall are 150 µm wide with a pitch of 350 µm.

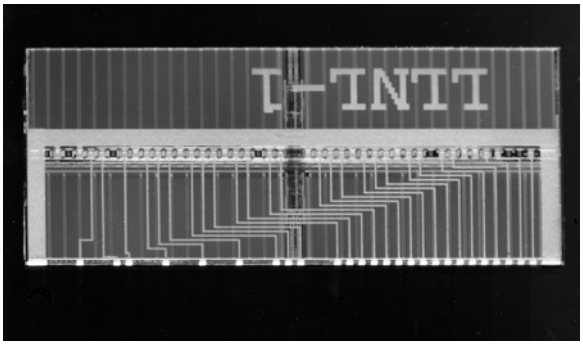

Figure 4 Pads near the die median of a 16 Mb DRAM chip have been rerouted to the edge of the die (visible at the bottom).

In order to eliminate solder bump attachment and reduce the complexity of both the flex and the substrate to which the stack is attached, the reroute pattern is not identical for all die. Address, power, ground, and some

control lines are identical but other control lines and all data lines are not. In Fig. 4, gaps are apparent between pads on the left hand half of the die. Successive die in the stack (labeled "LLNL-2", "LLNL-3", etc.) have data line pads on the side of the die offset with respect to those of LLNL-1 so that, while other lines on the various die will be connected to a common line on a flex tape (see below), each data line and certain control lines on each die will have their own I/O line on the flex. The various pad patterns can be seen clearly after the die are stacked, as shown in Fig. 5. The laser writing system easily accommodates the variation in the patterns to be written on the various die since only a change in the CAD file which drives the system is required. The cost benefits accrue from the reduction in the complexity of the next level of packaging.

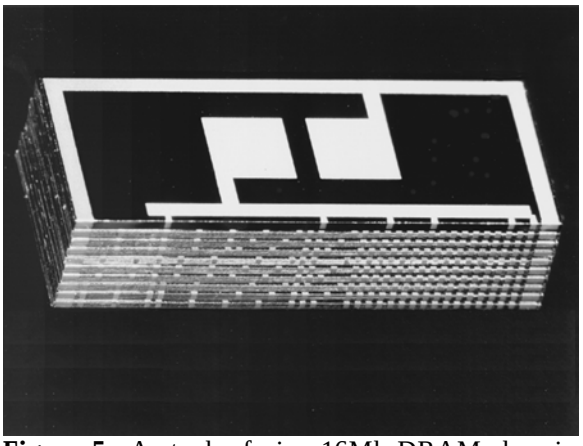

Figure 5: A stack of nine 16Mb DRAM showing the various side-wall pad configurations required for the memory architecture (see text). The top 'die' is simply a silicon substrate for mounting a decoupling capacitor.

Following reroute, die are removed from the carrier and stacked using a polyimide film adhesive. Die are aligned with respect to one another using a simple mechanical fixture. The alignment tolerances are not as severe for the flex attachment process as they are for solder bump attach. A modest misalignment caused by variations in the thickness of the die and the stacking adhesive could produce a substantial runout error if solder bumps are used. For our flex bonding scheme, however, there is no requirement for equal spacing between the die because pads are bonded to lines, not to individual pads. The orthogonal alignment tolerances are also fairly modest because the size and pitch of the sidewall pads are much larger than are needed for the ACA to be effective. Pads with pitch ≥ 0.004" can be successfully bonded.

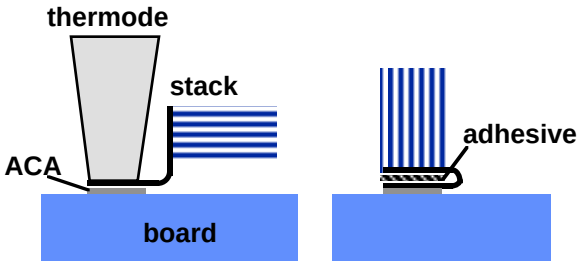

Figure 6 The final assembly step, following bonding of the flex tape to the circuit board with anisotropically conducting adhesive (ACA), is folding the flex over and bonding the back of the flex to itself.

The pads on the stack are bonded to the flex in a single step process using a diaphragm bonder. Approximately 60 PSI pressure is applied to the flex/ACA/stack through the thin aluminum diaphragm which seals one side of a nitrogen pressurized chamber. The entire assembly is heated to 140˚C for the 30 second duration of the bonding. A diaphragm bonder is used for stack-to-flex connection because the conformality of the nitrogen pressurized diaphragm provides equal force to the face of each die, assuring good contact to each die even if some are slightly misaligned.

In the final assembly (see Fig. 6) the flex circuit is bonded to the circuit board using a hot-bar thermode bonder. The PCB is heated to 60°C and the thermode is held at 150°C. A pressure of 100 PSI is applied for 30 seconds. After bonding, the flex tape is folded over and bonded to itself with an adhesive. The footprint of the stack plus flex is little more than the footprint of the stack itself.

Conclusions

A new method for packaging integrated circuits in three dimensions has been presented. The process utilizes a laser direct writing scheme to reroute I/O pads on DRAM chips to new pads on one of the long sides of the die. A vapor deposited polyimide coating or a PECVD SiO_2 layer is used as a dielectric passivation over the substrate and die, and an electrodeposited photoresist is patterned with a laser to form the interconnect image. The traces are plated with

copper to a thickness of 5 μm, and then covered with electrolytic nickel and gold for passivation and connection to the next packaging level.

Die are stacked and bonded, with pads arranged so that data lines in a stack are staggered but address are positioned identically. This architecture permits bonding of the stack to single sided flex tape in one operation using anisotropically conducting adhesive. The flex is bonded to the circuit board to complete the board assembly. Significant simplifications are achieved in this process.

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